REMARKS/ARGUMENTS

In the Office Action of 02/08/2005, the Examiner confirmed that Claims 1-58 are pending and that claims 48-58 are withdrawn from consideration, based upon Applicant's election in response to the Examiner's Restriction Requirement. The Examiner has allowed Claims 12 – 30 and 44 – 47; rejected claims 1 – 8, 10, 31 – 34, and 37 – 43; and objected to claims 9, 11, 35, and 36. The Examiner objected to the abstract in the specification, and accepted the drawings as filed.

In **Section 1** of the Detailed Action, the Examiner acknowledged applicant's election without traverse of the invention of group I, claims 1 – 47.

In view of the Examiner's earlier restriction requirement, Applicant retains the right to present claims 48 – 58 in a divisional application.

In **Sections 2 and 3**, the Examiner reminded Applicant of the requirements for an abstract of the disclosure and objected to the abstract because it exceeded 150 words. The abstract has been amended as required.

In **Sections 4 and 5**, the Examiner rejected claim 5 under 35 U.S.C. 112, second paragraph, stating that claim 5 contains the trademark/ trade name "FR-4". Although FR-4 is an industry designation of a fire resistant, general grade laminate made of woven fibreglass fabric saturated with an epoxy resin, Applicant has amended claim 5 to replace "FR-4" with the following descriptive words: "a fire resistant fiberglass dielectric material impregnated with epoxy resin."

In **Sections 6 and 7**, the Examiner rejected **claims 1 – 6, 8, and 10** under 35 U.S.C. 112 (b) citing US Patent Application Publication No 2002/0158335 to Towle et al. The Examiner took the position that Towle et al teach "an electronic package substrate for an electronic package (Fig. 1), comprising:

an adhesive bonding member (14) having two planar surfaces and an orifice there through for

receiving a chip (12); and

a circuitized member (16, 18) having two planar surfaces, one surface being bonded to one of the planar surfaces of the bonding member, said circuitized member being electrically connectable to the chip."

Towle et al describe the invention in paragraph [1013] as follows: "A [chip] is fixed within an opening in a package core to form a [chip]/core assembly. At least one metallic build up layer is then formed on the [chip]/core assembly and a grid array interposer unit is laminated to the assembly."

In referring to Fig. 1, Towle et al further explain in paragraph [0014]: "The [chip] 12 is fixed within an opening 24 in the package core 14 using an encapsulating material 22. ... [T]he metalization layer 16 is built up upon the [chip]/core assembly... The grid array interposer unit 18 is laminated to the [chip]/core assembly using any of a variety of different lamination techniques." In describing the package core 14, Towle et al state in the middle of paragraph [0019]: "The package core 14 can be formed from any of a variety of materials including, for example, bismaleimide triazine (BT), resin-based materials, flame retarding glass/epoxy materials (e.g., FR4), polyimide materials, ceramic materials, metal materials (e.g., copper), and others."

Claim 1 and **claims 2 – 6, 8, and 10**, which depend upon claim 1, specify "an *adhesive bonding* member" (emphasis added). The adhesive bonding member of applicant's invention has the properties of an adhesive and forms mechanical and chemical adhesive bonds to the circuitized member, as well as having structural properties.

There is no teaching or suggestion in Towle et al that package core 14 has any adhesive properties or that it can form any chemical or mechanical adhesive bonds to the circuitized member. Indeed, Towle et al teach that "the package core can be formed from ... ceramic material, metallic materials (e.g., copper), and others." Although Towle et al suggest that the package core 14 can be formed from bismaleimide triazine (BT), resin-based materials, or flame retarding glass/epoxy materials (e.g., FR4), it should be apparent that these materials would be fully cured before chip 12 "is fixed within an opening 24 in the package core 24 using an encapsulating material," [0014] since package core 14 could not be cured – at the temperatures and pressures required for curing – after

chip 12 is so fixed without substantial risk of damage to chip 12 or its connections. The package core 14 taught by Towle et al is just that – a package core and not an adhesive bonding member. Towle et al teach away from package core 14 being or acting as an adhesive bonding member or having any adhesive properties.

The Examiner took the position that the combination of Towle's metalization layer 16 and the grid array interposer unit 18 constitute or are equivalent to applicant's circuitized member. Towle et al teach that "the metalization layer 16 is built up upon the [chip]/core assembly" [0014] – not bonded to or by an adhesive bonding member. The techniques for building up a metallic layer on a core or a substrate are quite different from using an adhesive member. Towle et al teach that "The grid array interposer unit 18 is laminated to the [chip]/core assembly using any of a variety of different lamination techniques." Although Towle et al do not specifically call out using a thin layer of adhesive paste or illustrate in any of the figures a thin layer of adhesive paste, Towle et al imply or suggest that a thin adhesive paste is used to bond the grid array interposer unit 18 to the metalization layer 16. In the middle of paragraph [0029] state that: "In an alternative approach, the solder mask could be patterned across the active surface and simultaneously act as an adhesive for attachment of the interposer." A thin layer of adhesive paste applied to join the grid array interposer unit 18 to the metalization layer 16 is not a bonding member having two planar surfaces and an orifice there through for receiving a chip. Likewise, a solder mask that acts as an adhesive for the attachment of the interposer to the [chip]/core assembly on which a metalization layer has been built up is not a bonding member having two planar surfaces and an orifice there through for receiving a chip. Towle et al teach that "[t]he [chip] is fixed within an opening 24 in the package core 14..." not within an orifice of a bonding member. Neither a thin layer of adhesive paste nor a solder mask present an orifice for receiving a chip.

Applicant has amended claim 1 by adding the words: "said bonding member prior to assembly of the electronic package substrate being a stiff sheet of adhesive that is substantially not sticky and after curing said bonding member having mechanical and chemical adhesive bonds with the circuitized member" to more clearly specify the adhesive bonding member. The antecedent basis for this amendment is in [0085]. Applicant believes that Claim 1 as presently amended is patentable.

Claim 2 has been cancelled.

Regarding **claim 3**, the Examiner has taken the position that Towle et al "teach an electronic package substrate, wherein the bonding member is a structural support for the substrate."

As pointed out above, the package core 14 of Towle et al is not an adhesive bonding member and there is no suggestion that the package core act as an adhesive bonding member.

Applicant has amended claim 3 to more clearly specify the structural support and the purpose and benefit therefrom, by adding the following underlined words "after curing the electronic package substrate, the mechanical and chemical adhesive bonds between the bonding member and the circuitized member, as well as the bonding member itself, [[is]] together act as a structural support to absorb the stress and strain subjected to [[for]] the substrate." The support for the changes is in [0085] – [0086]. Applicant believes that Claim 3 as presently amended is patentable.

Regarding **claims 4 – 6**, the Examiner has taken the position that Towle et al "teach an electronic package, wherein the bonding member is fabricated from a glass-fiber-reinforced/filled epoxy resin"... "from FR-4" ... "from BT resin."

The package core 14 of Towle et al, including one made from a glass-fiber-reinforced/filled epoxy resin, from FR-4, or from BT resin, is not an adhesive bonding member and there is no suggestion that the package core act as an adhesive bonding member or that any adhesive that might be incorporated into the package act as a structural support. To serve as a package core 14 in the [chip]/core assembly of Towle et al, the glass-fiber-reinforced/filled epoxy resin, the FR-4, and the BT resin suggested by Towle et al would need to be used in a cured state in which the glass-fiber-reinforced/filled epoxy resin, the FR-4, and the BT resin would have no adhesive or bonding properties.

Claim 4 has been amended to more clearly define and specify the bonding member by making the following changes: "wherein the bonding member prior to bonding to the circuitized member is ~~fabricated from~~ a stiff sheet of B-stage cured glass-fiber-reinforced/filled epoxy ~~resin~~ adhesive." The antecedent basis for this amendment is in [0085]. Applicant believes that Claim 4 as presently amended is patentable.

Claim 5 has been amended in response to the Examiner's assertion that FR-4 is a trademark

or trade name to replace the term "FR-4" with the words: "a fire resistant fiberglass dielectric material impregnated with epoxy resin." The antecedent basis for this amendment is in [0085]. Applicant believes Claim 5 is patentable because it depends from Claim 4, and Applicant believes that Claim 4 as presently amended is patentable. Although Towle et al teach the use of FR-4 as a package core, Towle et al neither teach nor suggest using FR-4 as an adhesive. Applicant respectfully requests that the Examiner remove the rejection and objection and allow Claim 5.

Applicant has resubmitted **Claim 6** in its original form. Applicant believes Claim 6 is patentable as originally submitted for the following reasons. Claim 6 depends from Claim 4, and Applicant believes that Claim 4 as presently amended is patentable. Although Towle et al teach the use of BT resin as a package core, Towle et al neither teach nor suggest using BT as an adhesive. Applicant respectfully requests that the Examiner remove the rejection and allow Claim 6.

Regarding **claim 8**, the Examiner took the position that "Towle et al. teach an electronic package substrate, wherein the bonding member is electrically conductive."

While Towle et al admittedly teach that the package core 14 can be formed from metal materials and that in one illustrated embodiment "the package core 14 is formed from a dielectric board material ... having a conductive cladding 20" [0019], the package core 14 of Towle et al is not an adhesive bonding member and there is no suggestion that package core 14 act as an adhesive. Towle er al do not teach and provide no suggestion that any adhesive be electrically conductive.

Applicant has resubmitted **Claim 8** in its original form. Applicant believes Claim 8 is patentable because it depends from Claim 1, and Applicant believes that Claim 1 as presently amended is patentable, and because Towle et al neither teach nor suggest using an electrically conductive adhesive as a bonding member or as a means to bond a package core to a circuitized member. Towle et al teach using a package core with a conductive cladding, but that teaches away from using a package core as an adhesive. In view of the foregoing the Applicant respectfully requests that the Examiner remove the rejection and allow claim 8.

Claim 10 has been cancelled.

In **Section 8**, the Examiner rejected **claims 31 – 33, 37, and 39** under 35 U.S.C. 102 (b) as

being anticipated by US Patent No 6,488,806 to Carden et al.

Regarding **claims 31 and 33**, the Examiner took the position that "Carden et al. teach an electronic package (Fig. 4), comprising:

an adhesive bonding member (10) having two planar surfaces and an orifice there through;

a circuitized member (2) bonded to one of the planar surfaces and blocking the orifice, thereby forming a cavity for receiving a flip chip (4); and

Carden et al. inherently teach an array of solder pads on the circuitized member, since they would be required for the array of solder balls (6)."

Carden et al show an adhesive 10 in Figures 2, 3, and 4. The only reference to adhesive 10 in the specification is at column 3, lines 38 – 40: "The cross-sectional view of FIG. 2 shows stiffener 8 is attached to laminate chip carrier 2 preferably by adhesive 10." Carden et al refer to the use of a stiffener with a laminate chip carrier in the BACKGROUND at column 1, lines 34 – 40: " ... packages frequently include a conductive stiffener mounted on the laminate chip carrier and a cover plate mounted on the chip. The stiffener, usually comprised of metal, is preferably mounted onto the laminate chip carrier such that the stiffener surrounds the perimeter of the chip ..." In the SUMMARY OF THE INVENTION, Carden et al again refer to the stiffener-chip carrier combination at column 2, lines 9 – 12: "providing a laminate dielectric chip carrier ... and preferably a stiffener mounted onto a portion of the laminate chip carrier mounting a chip onto the laminate chip carrier ..." In claim 11, Carden et al refer to the stiffener-chip carrier combination in the preamble of the claim: "A method of making a flip-chip package having a laminate chip carrier with a stiffener attached thereon ..." The only reasonable inference is that adhesive 10 is a thin layer of paste used in prior art techniques for mounting one member on another member or attaching two members together.

Claims 31 and 33 of the present application recite "an adhesive bonding member" – not an adhesive paste. Figure 12 of the present application shows a bonding member 430. Bonding member 430 is substantially thicker than circuitized member 428. Applicant's flip chip package substrate "comprises a relatively thin, flexible circuitized member bonded to a relatively thicker, substantially rigid bonding member." [0162] Applicant differentiated and distinguished the bonding member from

the prior art paste in [0163], "the primary bonding member in the flip chip package substrate is not merely a thin layer of adhesive, but is a structural member of the flip chip package substrate and forms the walls of the cavity into which a flip chip is placed." The material used to make bonding member is further described in [0172]: "The glass fiber reinforced/filled epoxy adhesive initially is introduced into the process of making flip chip package substrates 426, as a solid sheet, or as a laminate of solid sheets, of the adhesive in a partially cured or "B-stage" cured condition.... The glass fiber reinforced/ filled epoxy adhesive, such as FR4, in a B-stage cured condition, is relatively stiff, not sticky, relatively stable, and relatively easy to handle. In the bonding and curing process, the glass fiber reinforced/filled epoxy adhesive flows sufficiently under higher temperatures and pressures to fill in gaps, forms mechanical and chemical bonds with circuitized member 428, ..."

Carden et al taught the use of a conventional thin adhesive paste to attach a stiffener to a laminate chip carrier or circuitized member. The adhesive disclosed by Carden et al does not provide or form a cavity for a flip chip and does not become a stiffener for a flip chip package. Carden et al teach using a separate and preferably metal member to act as a stiffener and to provide a cavity for the flip chip. The present invention teaches using a relatively stiff, adhesive bonding member that bonds to the circuitized member, acts as a stiffener, and provides a cavity for the flip chip.

Claims 31 and 33 have been amended to more clearly define and specify the bonding member by adding the words: "said bonding member prior to assembly of the electronic package substrate being a stiff sheet of adhesive that is substantially not sticky and after curing said bonding member having mechanical and chemical adhesive bonds with the circuitized member." Applicant believes claim 31 and claim 33 are patentable as presently amended for the reason stated above.

Regarding **claims 32 and 37**, the Examiner took the position that "Carden et al. teach a package, further including a stiffening member (8) and having an orifice there through overlying the orifice in the bonding member."

Carden et al recite as prior art "to increase thermal dissipation and flatness of the flip-chip package, the packages frequently include a conductive stiffener mounted on the laminate chip carrier..." [column 1, lines 34 – 36] Carden et al teach that "Stiffener 8 [in their flip-chip package] provides a counter force to laminate chip carrier 2 and assures dimensional stability of the flip-chip

package when the laminate chip carrier 2 may tend to bow, twist or warp during thermal cycling as a result of the difference in the CTE between the laminate chip carrier 2 and chip 4."

Applicant has **amended claims 32 and 37**, adding the words: "said stiffening member providing an additional structural support to the substrate in addition to the mechanical and chemical adhesive bonds and bonding member itself" to clarify that the stiffening member provides supplemental structural support in addition to the support provided by the bonding member and not the primary support. Applicant has further amended claim 32 to insert the words: "electronic package" before the word "substrate" for more consistent use of terminology. Applicant has further amended claim 32 by making claim 32 depend from new claim 59, which in turn depends from claim 31, rather than depending directly from claim 31. Applicant submits that claim 32 and claim 37 as presently amended are patently distinguishable from Carden et al and are patentable.

Claim 39 has been cancelled.

In **Sections 9 and 10**, the Examiner rejected **claim 7** under U.S.C. 103(a) as being unpatentable over Towle et al as applied to claim 1 and further in view of US Patent No, 6,734,535 to Hashimoto.

Claim 7 has been cancelled.

In **Section 11**, the Examiner rejected **claim 34** under U.S.C. 103(a) as being unpatentable over Carden et al in view of admitted prior art. The Examiner took the position that Carden et al teach a package further including an array of solder bumps (6), which would have included solder pads. The Examiner also took the position that admitted prior art teaches that it is typical in the art to use solder having a melting temperature above 215 degrees Celsius, or more specifically above 225 – 235 degrees and that it would have been obvious to one of ordinary skill in the art to incorporate the teaching of admitted prior art into the device taught by Carden et al.

Applicant has amended claim 34 by adding the words: "wherein the adhesive bonding member and the circuitized member are made from organic materials and" to clarify that claim 34 is directed to an electronic package for a flip chip in which the adhesive bonding member and the circuitized

member are made from organic materials. Applicant has further amended claim 34 by changing the temperature from 215°C to 225°C to conform the temperature in the claim to the temperature specified in paragraphs [0029] and [0178] of the specification, wherein the subject is discussed.

Applicant believes that claim 34 as amended is patentable for the following reasons. As Applicant stated in the specification, organic materials, such as FR-4, BT resin, and other glass-fiber-reinforced/filled epoxy resins, "have a glass transition temperature of about 150°C to about 170°C, a temperature above which the materials begin to soften, and a breakdown temperature of about 225°C to about 235°C, a temperature above which the materials can char or begin to burn. These organic materials will be damaged if exposed to temperatures above 225°C - 235°C for a sustained time period." [0023] Applicant further noted "the melting temperature of the solder bumps (or other electrically conductive bumps) on flip chips typically is substantially greater than 225°C - 235°C." [0028] In the conventional process for melting and attaching solder bumps on a flip chip to a flip chip package substrate, the temperature in a conventional reflow generally is raised above 225°C - 235°C. Since materials used to make flip chip package substrates must be able to withstand temperatures that are higher than 225°C - 235°C, organic materials have effectively and economically been ruled out for making flip chip package substrates. [0028 – 0029] In the prior art flip chip package substrates used for flip chips that have solder bumps that melt at temperatures greater than 225°C have been made of ceramic materials. [0029] "Melting and fusing solder bumps that are made from a solder material that has a melting temperature above 225°C to a laminate of multiple layers of epoxy might degrade the laminate of multiple layers of epoxy, especially if the solder bumps are melted and fused by the methods currently used in the industry." [0178] It is Applicant's unique process for attaching solder bumps on a flip chip to a flip chip package substrate, illustrated in Figure 16 and described in paragraphs [0186] through [0193] that enables organic materials to be used as an adhesive bonding member in a flip chip package substrate used for flip chips that have solder bumps that melt at temperatures greater than 225°C. Applicant teaches that "using an induction heater to attach flip chip 422 to flip chip package substrate 426, makes it possible to use organic materials, such as FR4 or BT-resin, in flip chip package substrate 426, without risk of damaging flip chip package substrate 426 during the attachment process." Prior art teaches away from using

organic materials in flip chips that have solder bumps that melt at temperatures greater than 225°C. [0029]

In **Section 12**, the Examiner rejected **claim 38** under U.S.C. 103(a) as being unpatentable over Carden et al as applied to claim 33 and further in view of Towle et al.

Claim 38 has been cancelled.

In **Section 13** of the Office Action the Examiner explicitly rejected **claims 40 – 42** and implicitly rejected **claim 43** under 35 U.S.C. 103 as being unpatentable over Carden et al. in view of US Patent No. 6,472,762 to Kutlu. (Since the Examiner refers to claim 43 in the last paragraph of Section 13, along with claim 42, Applicant infers that the listing of claims in the first sentence of Section 13 was intended to include a rejection of claim 43.)

Claims 40 and 41 have been cancelled.

Regarding claims 42 and 43, the Examiner acknowledged that Carden et al. do not teach a package including an electrical ground plane formed by an electrically conductive heat sink and an electrically conductive bonding member, both connectable to ground. The Examiner took the positions that Kutlu teaches a package including an electrical ground plane formed by an electrically conductive heat sink and an electrically conductive bonding member, and that the electrical ground plane could also function as a shield since it is connectable to ground. The Examiner further stated that it would be obvious to incorporate the teaching of Kutlu into the device taught by Carden et al. since it is desirable to remove excess heat from the die.

Carden et al. states at Column 3, Lines 38 – 40 "The cross-sectional view of FIG. 2 shows stiffener 8 is attached to laminate chip carrier 2 preferably by adhesive 10." This is the only reference to adhesive 10 and the only reference describing how stiffener 8 is attached to chip carrier 2.

Kutlu states: "The package 100 may be implemented as an enhanced laminate flipchip package using a heatspreader with a high coefficient of thermal expansion (CTE).... The coefficient

of thermal expansion (CTE) of the die 102 and the heatspreader 104 combination may be adjusted to match the CTE of the substrate 106." (Column 2, Lines 48 – 51; column 2, lines 56 –59) Kutlu further states: "The die attachment material 108 may be implemented as a high modulus, high glass transition temperature (Tg) adherent (e.g., an epoxy, a metal alloy, etc.)." (Column 3, lines 6 – 8) Kutlu continues his description: "The CTE of the die 102 is generally lower than the CTE of the substrate 106. The heatspreader 104 generally has a CTE that is greater than the CTE of the substrate 106. One or more characteristics of the heatspreader 104 may be adjusted to provide an effective CTE of the combination of the die 102 and the heatspreader 104 substantially the same as (matches) the CTE of the substrate 106." (Column 3, lines 25 – 31)

Claim 42, which depends from Claim 33, recites "an electrical ground plane formed by an electrically conductive heat sink and by an electrically conductive bonding member, both connectable to ground".

Claim 43, which also depends from Claim 33, specifies "a shield against electromagnetic interference formed by an electrically conductive bonding member, an electrically conductive second bonding member, and an electrically conductive heat sink, all electrically connectable to ground".

Applicant has resubmitted Claims 42 and 43 without amendment. For the reasons set forth below the Applicant believes that Claims 42 and 43 are patentable as originally submitted.

Claims 42 and 43 depend from Claim 33 and the Applicant believes that Claim 33 as presently amended is patentable.

In the Office Action the Examiner indicated that it would be obvious to incorporate the teaching of Kutlu into the device taught by Carden et al. since it is desirable to remove excess heat from the die. While Applicant can hardly deny in the abstract that it is desirable to remove excess heat from the die, Applicant respectfully submits that there is no teaching, suggestion, or even a hint in those references to combine them together. Further, Carden et al. and Kutlu are each solving different problems and there is no motivation to bring them together. The Examiner's attention is directed to Section 2143.01of the MPEP.

In addition, Carden et al. and Kutlu teach the use of a metallic heat sink for its thermal

capabilities and not for its electrical properties. Applicant can find no description in Carden et al or in Kutlu of any structure that would allow the metallic heat sink to utilize its properties as an electrical conductor, or one that can form an electrical ground plane for the chip.

Further, Applicant can find no teaching in either Carden et al. or Kutlu that teaches how to electrically connect the metallic heat sink to the electrical ground of the chip and how such a structure would then function as a ground plane or as an effective EMI shield. In contrast, Applicant has disclosed and claimed an electrically conductive adhesive bonding member bonded to the electrically conductive heat sink and electrical paths from the heat sink to the ground of the chip and grounded solder balls on the electronic package.

In view of the foregoing the Applicant respectfully requests that the Examiner remove the rejection and allow Claims 42 and 43.

In **Sections 14 and 16**, the Examiner allowed **claims 12 – 30 and 44 – 47** and gave his reason therefore.

In **Section 15**, the Examiner objected to **claims 9, 11, 35, and 36** as being dependent upon a rejected base claim, and stated that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 9, 11, 35, and 36 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant has added new **claims 59 and 60.**

Claim 59 depends from claim 31. Claim 31 has been amended and Applicant believes that claim 31 as amended is patentable. The antecedent basis for the additional limitations in claim 59 is described in paragraphs [0172], [0174], [0182], and [0086].

Claim 60 depends from claim 33. Claim 33 has been amended and Applicant believes that

claim 33 as amended is patentable. The antecedent basis for the additional limitations in claim 60 is described in paragraphs [0172], [0174], [0182], and [0086].

In view of the above, it is submitted that the claims pending in this application are now in condition for allowance. Applicant respectfully requests that the Examiner reconsider and withdraw his rejections and objection and allow claims 1 , 3 – 6, 8, 9, 11, 31 – 37, 42, and 43, and consider and allow new claims 59 – 60, and to pass the application to issue.

If in the Examiner's opinion this case can be moved to issue more expeditiously through a telephone discussion, the Examiner is invited to call Applicant's attorney at the telephone number below.

Respectfully submitted,

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